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a light reception step of receiving light introduced into said elements of said optical area and photoelectrically converting the light;

an arithmetic operation step of arithmetically operating a plurality of signals in parallel obtained for each of said elements by the photoelectric conversion of the processing in the light reception step in accordance with a predetermined rule;

an outputting step of outputting a result of the arithmetic operation of the processing in the arithmetic operation step for each of said elements; and

a timing adjustment step of adjusting a timing at which the result of the arithmetic operation is to be outputted for each of said plurality of elements by the processing in the outputting step.

#### REMARKS

In the Office Action, claims 1-10 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,166,583 ("*Kochi*"). Applicant respectfully submits that this rejection has been overcome in view of the amendments and/or for the reasons set forth below.

Of the presently pending claims, claims 1 and 6 are the sole independent claims. Independent claims 1 and 6 have been amended. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made.**"

Claim 1 relates to an image processing apparatus that has an optical area in which a number of elements are disposed in a matrix. The image processing apparatus includes a light reception means for receiving light introduced into the elements of the optical area and photoelectrically converting the light; and arithmetic operation means includes a number of arithmetic operating units, each of which operates a signal obtained for one of the elements by the photoelectric conversion by the light reception means in accordance with a predetermined rule; and outputting means for outputting a result of the arithmetic operation of the arithmetic means for each of the elements; and timing adjustment means for adjusting a timing at which the result of the arithmetic operation is to be outputted for each of the elements from the outputting means.